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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,207	07/29/2003	Theodore Carter Briggs	200312685-1	1123

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EXAMINER

BAKER, STEPHEN M

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/632,207

Applicant(s)

BRIGGS ET AL.

Examiner

Stephen M. Baker

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 072903.022205.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 1, in line 14, "Error codes" apparently should be "Error control codes".

On page 1, in line 16, "codes" apparently should be "control codes".

On page 1 in line 17, "or check bits can" apparently should be "also called check bits, can".

On page 1, in line 18, "error or correction" apparently should be "check".

On page 1, in line 29, "provided" apparently should be "provides".

On page 1, in lines 31-32, "An error correction code (ECC) consists of a group of bits, or codes, associated with a piece of data." apparently should be deleted, as two other terms besides "codes" have already been used by applicant to describe error control code redundancy, and as "codes" is most often used by practitioners synonymously with "codewords".

On page 2, in line 3, "based on" apparently should be "confined within" or the like.

On page 2, in lines 6-7, "failure of an entire DRAM chip during a DRAM cycle (e.g., read operation, write operation) organized into a 4-bit width configuration" apparently should be "failure of an entire 4-bit wide DRAM chip during a DRAM cycle (e.g., read operation, write operation) in a configuration"

On page 2, in lines 22-23, "partitioned into separate adjacent bit pair domains, such that a single adjacent bit pair from each memory device is assigned to a given domain" is unclear and apparently should be "partitioned into domains referred to herein as 'adjacent bit pair domains,' with each adjacent bit pair domain being assigned an adjacent bit pair from each memory device" or the like.

On page 3, in lines 26-28, "process data structures with more bits than can be detected and corrected by the ECC techniques employed" apparently should be "process data structures having more bits than can be detected and corrected by a single application of the ECC techniques employed" or the like.

On page 3, in lines 28-30, "partitioning a data block and/or data structure into separate domains equal to the number of bits that can be processed by the ECC technique" apparently should be "partitioning the data structure (data block) into domains having a number of bits equal to the number of bits that can be processed by a single application the ECC technique" or the like.

On page 3, in line 30, "achieved" apparently should be "facilitated" or the like.

On page 4, in line 13, "#K, where K is an integer greater than one" apparently should be "#K".

On page 4, in lines 14-15, "be for example, but not limited to" apparently should be "be, for example but not limited to".

On page 4, in line 21, "width columns" apparently should be "column width".

On page 4, in lines 22-23, "an ECC checker and corrector for a 288 bit data structure would be impractical" apparently should be "an ECC checker and corrector for a 288-bit ECC codeword is considered impractical" or the like.

On page 4, in line 25, "devices" apparently should be "device".

On page 4, in line 28, "sequentially or in parallel" apparently should be "sequentially in less time than otherwise required, or in parallel" or the like.

On page 5, in lines 10-11, "The adjacent bit pair domains are populated with the check bits and data bits from the data block" apparently should be "The check bits for the data block are then added to the adjacent bit pair domains" or the like.

On page 5, in lines 11-12, "The adjacent bit pair domains are assigned adjacent data bit pairs per memory device" apparently should be "The adjacent bit pair domains are assigned to adjacent data bit pairs for each memory device" or the like.

On page 6, in line 3, "correctable by the error corrector" apparently should be "correctable within a desired amount of time by the error corrector" or the like.

On page 6, line 27, "facilitate speed associated with" apparently should be "facilitate faster" or the like.

On page 6, in line 28, "additional check bit" apparently should be "additional ECC codeword check bit" or the like.

On page 6, line 30, "facilitate speed associated with" apparently should be "facilitate faster" or the like.

On page 6, in line 33, "provides chipkill" apparently should be "facilitates chipkill" or the like.

On page 7, in line 3, "K, where K is an integer greater than one" apparently should be "#K".

On page 7, in line 34, "#K, where K is an integer greater than one" apparently should be "#K".

Correction of the remaining errors is left to applicant.

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. 10/632,206. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present claims are seen as essentially a re-hash of claims 1-25 of copending Application No. 10/632,206 with the

exception that the present claims do not recite transferring both bits of each adjacent bit pair on a same path.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Stephen M. Baker
Primary Examiner
Art Unit 2133

smb